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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,254	12/08/2000	Elana D. Granston	TI-29189	3119
23494	7590	04/22/2004	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			VU, TUAN A	
			ART UNIT	PAPER NUMBER
			2124	
DATE MAILED: 04/22/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/733,254	GRANSTON ET AL.
	Examiner Tuan A Vu	Art Unit 2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 29 January 2004.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-4 (claims 5-6 canceled) is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-4 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 08 December 2000 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date. _____.   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

## **DETAILED ACTION**

1. This action is responsive to the Applicant's response filed 1/29/2004.

As indicated in Applicant's response, claims 1, 4 have been amended and claims 5,6 canceled. Claims 1-4 are pending in the office action.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential clarification steps as to help defining the metes and bounds of a specific limitation.

The limitation recited as 'without special hardware support or special loop control instruction' (line 4) is not defined in terms so to enable a clear interpretation about what constitutes an action that is being based on not needing some other elements. In other words, the claim does not sufficiently support how the step of 'determining' (line 1) as claimed is being performed without some steps or other elements, i.e. stating that an action is not taken, or that a feature is not there does not specify the scope of an inventive step. The examiner will interpret this 'without' limitation as loosely as if such limitation had no weight.

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitation recited as ‘without special hardware support or special loop control instruction’ (line 4) is not described anywhere in the specification. About determining which instructions are to be done via speculation, it is noted that pg. 9, and especially pg. 10 (top) relate to what is done when speculation is to be determined and subsequently executed; however, there is no mention of special hardware support nor is there any mention of special loop control instructions.

*Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rau et al., “Code Generation Schema for Modulo Scheduled Loops”, ACM Proceedings of the 25<sup>th</sup> annual International Symposium on Microarchitecture, Dec 1992, volume 23, iss. 1-2, (hereinafter Rau\_1), in view of Rau et al., “Register Allocation for Software Pipelined Loops”, June 1992, In Proc. of the ACM SIGPLAN'92 Conference on Programming Language Design and Implementation, pages 283-299 (hereinafter Rau\_2), and further in view of Akkary, USPN:

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6,240,509 (hereinafter Akkary) and Bringmann, "Enhancing Instruction Level Parallelism through compiler-controlled speculation", Univ. of Illinois, 1995 (hereinafter Bringmann).

**As per claim 1,** Rau\_1 discloses a method for pipelining program loops having irregular loop control comprises the steps of:

determining which instructions in loop code in a memory may be speculatively executed (e.g. pg. 161, ch. 2.3; pg. 163, ch. 3.1, 3.2);

storing in a computer memory a set of registers (e.g. pg. 161, ch. 2.1; *rotating registers* - pg. 164, ch. 3.4; pg. 169, Fig. 9-11).

But Rau\_1 does not explicitly disclose that the determining of loop instructions for speculation execution is without special hardware support and special loop instructions. Rau\_1 discloses analysis of branch operations and control dependencies thereof and determination upon which instructions can be speculatively executed (pg. 16, ch. 1.5). The concept of using compiler-supported techniques or data profiling to support speculation of loop operations involving branch prediction was a known concept in the art of loop scheduling and optimizations at the time the invention was made. In a disclosure analyzing how to apply save speculation using ILP, loop unrolling, block analysis, dependence graph, variable extension techniques analogous to the modulo scheduling approach by Rau\_1 (Rau\_1: *dependence graph* - pg. 158-159, ch. 1.2; 1.3), Bringmann discloses many compiler-controlled techniques to help applying save speculation in a loop scheduling optimizing method (ch. 3, 4, 5), thus without hardware support in the process of determining what instructions to speculate. Just in case Rau\_1 does not already use similar compiler techniques to support speculation determination as mentioned in the above ILP-based Modulo scheduling process, it would have been obvious for one of ordinary

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skill in the art at the time the invention was made to apply compiler-aided techniques such as dependency graph, operand inspection, superblock dependency removing, algorithms, etc. as taught by Bringmann ( i.e. without special hardware support and special loop instructions) so to effect this speculation determination because of immediacy and criticality of such determination at compile time when hardware exertion, e.g. register pressure, in many architectures in such time is a serious constraint and that critical path dependency and branch resolution has to be expedited in order to obviate costly potential execution exceptions.

Further, Rau\_1 does not explicitly disclose storing a set of registers that are modified by an instruction and are alive out of the loop but suggest use of virtual register and extension of variables (pg. 159, ch. 1.3). Rau\_2, in a method to support the pipelining of loops and control thereof, discloses a form of extending registers utilization analogous to Rau\_1 and further provides keeping of registers that are modified by an instruction and alive out of the loop iteration ( e.g. *register allocator* , *loop-variant*, *virtual register*, *live-in*, *live-out*, *scalar lifetime*, *vector lifetime* - pg. 284-286, ch. 1.3 – Note: the allocation of register in conjunction with determining of loop related variants is equivalent to storing registers modifiable by loop instructions). It would have been obvious for one of ordinary skill in the art at the time the invention was made to provide the loop-related live register monitoring or recording as taught by Rau\_2, in case Rau\_1 does not already include one such process, because this would enable the allocation of registers in more effective and resource-oriented fashion in keeping pace with variables being changed as a result of a loop iteration or pipeline kernel/stage completion, given the constraint associated with architectural limited number of registers.

Nor does Rau\_1 disclose modifying the program code so that the values of those registers are saved to a temporary register during all proper iterations; and copying back to the register the value of the temporary register once the loop is completed. Rau\_1, however, suggests hardware support for 2 copies of operations in case of exception mishaps during speculation ( pg. 161, ch. 2.3) and suggests use of virtual registers (pg. 159, ch. 1.3). In a method using speculation in handling pipelined loops analogous to that of Rau\_1, Bringmann discloses register extensions ( pg. 52, ch. 4.3.2) and Akkary discloses the use of temporary registers and instruction trace buffer for execution of the speculation-intensive pipeline in order to prevent mis-speculation recovery resources (e.g. Fig. 12-16; col. 11, line 60 to col. 12, line 22); hence teaches the committing or copying of values to and from secondary registers to provide for mishaps recovery and rollback situations from the course of taking a wrong path during execution. When register resources are available, it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement to 2-copies techniques with hardware support by Rau\_1 ( enhanced by Rau\_2) the use of register support such as register extension by Bringmann, or temporary registers as taught by Akkary, because this would allow extended means to provide for mishaps recovery and rollback situations from taking a mistaken path during loop execution or speculative operation, so to make optimal use of architectural resources as intended by both Rau\_1 and Rau\_2.

**As per claim 2 and 3,** Rau\_1 teaches minimizing the latency due to initiation interval between iterations, applying the optimization with intent reduce to kernel-only pipelines ( e.g. pg. 158-160; *kernel-only* – pg. 164, ch. 3.5), hence has implicitly disclosed downsizing to loop pipelining ( re claim 2) with a minimum trip count being reduced to 1; further, Rau\_1 discloses

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one structure pipeline of loop to which modulo schedules is applied (e.g. pg. 158-160), hence has implicitly disclosed elimination ( re claim 3) of multi-version loop code.

**As per claim 4,** Rau\_1 discloses a method for software pipelining of irregular conditional control loops, the method including pre-processing the loops so they can be safely pipelined, comprising:

- pre-processing each instruction in the loop in turn (e.g. *loop-variant, basic block, unrolling, modulo scheduling, dependence graph* -- pg. 158-159, ch. 1.2;);
  - if the instruction can be safely speculated, leaving it alone (e.g. pg. 163-164, ch. 3.1, 3.2
    - Note: speculation can be executed without additional need to set up for predicated instruction is equivalent to let speculative execution alone);
  - pre-processing the instruction using predication (e.g. pg. 161, ch. 2.2; pg. 164, ch. 3.4-3.5
    - Note: predication such as If-conversion using control register implicitly discloses an alternate means to using speculative execution because the former requires additional setting resources compared to the latter).

But Rau\_1 does not explicitly disclose pre-processing of instructions that modify registers that are live out of the loop. But Rau\_1 teaches register use for iteration control ( pg. 161, ch. 2.1-2.2) hence has implicitly taught a certain level of instruction analysis in conjunction with modifying contents of a register. The limitation as to use analysis on alive register out of a loop has been addressed in claim 1 using Rau\_2 using the rationale that analyzing of live registers would enhance the saving of resources while allocating of registers during the process of minimizing resources reuse and variables overlapping across iterations of pipelined loops.

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Nor does Rau\_1 disclose register copying as a prior alternate to applying predication, upon determining that an instruction modifies registers as seen above. But in view of the teachings as to make 2 copies of operations by Rau\_1, to anticipate conflicts from unsafe speculation by extending registers by Bringmann, and to allocate temporary storage like buffers and registers by Akkary as earlier mentioned in claim 1 above, the use of register copying as a first step to do before any speculative execution would have been obvious because of the urgency of taking preventive measures over recovery measures and because of the additional reasons set forth in corresponding rationale used in claim 1.

***Response to Arguments***

8. Applicant's arguments filed 1/29/2004 have been fully considered but they are not persuasive.

As per claim 1, Applicants have submitted that Rau\_1 relies on hardware for speculative execution or speculative code motion (Appl. Rmrks, pg. 7, 2<sup>nd</sup> para). The claim recites determining whether instructions can be speculated without hardware support; and does not recite any limitation that enforces speculative execution without using hardware support; hence Applicants has argued upon a feature not claimed. Besides, the claim does not establish explicit description as to how the speculation determining process is being done without hardware support.

Applicants have submitted that Rau\_2 and Akkary disclose sized-extensive MVA, or non-trivial use of buffers, respectively (Appl. Rmrks, pg. 7, 3<sup>rd</sup> and 4<sup>th</sup> para). The use of temporary storage and securing therein data needed in case of rollback or recovery from exception have been the reasons stated in the rejection; and the reasons mentioned by Applicants

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seem to coincide with the rationale as set forth therein. Hence, a case of Prima Facie has been established when the rejection shows that Rau\_1 suggests a duplicating method, that Bringmann teaches extension of registers, and Akkary uses of temporary buffers, all of which approaches suggesting preventive measures to restore a failing system or to obviate a mistaken path conflict. Hence, Applicants have failed to establish how the combination and the rationale used in the rejection teach away from or are at odds with what Applicants believe to be the invention.

As per claim 4, Applicants' arguments revolve around the same issue of temporary registers; and such issue has been addressed above in light of the rejection.

Therefore, the claims are rejected as it now stands in the rejection.

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(703) 872-9306 ( for formal communications intended for entry)

**or:** (703) 746-8734 ( for informal or draft communications, please consult Examiner before using this number)

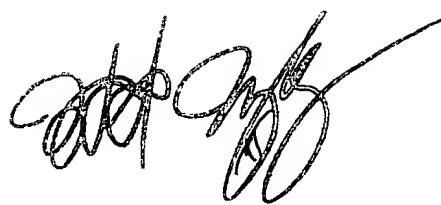
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4<sup>th</sup> Floor( Receptionist).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT  
April 17, 2004

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**PRIMARY EXAMINER**